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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,230	04/08/2004	Mark B. Fuselier	2000.092182	9406

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,230	FUSELIER ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30,56-61 and 74-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30,56-61 and 74-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-30 and 74-79 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the disclosure for a device comprising an area defined by one (an) isolation structure formed in the active layer, as recited in claims 77-79.

There is no support for the claimed limitations of "said doped back gate region extending under an entirety of said multiple thickness buried oxide layer between said isolation structure", as recited in claims 1, 13, 23 and 77-79.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-30, 56-61 and 74-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (6,096,582) in view of En et al. (6,611,023). Regarding claims 1-3, 5, 7-9, 13-14, 16, 18-19, 23, 25, 27 and 77-79, Inoue et al. teach in figure 2 and related text a transistor comprised of a channel region, said transistor comprising:

a bulk silicon substrate 1 and a silicon active layer 2, 3, 4;

an isolation structure 82" (see figure 17A) formed in said active layer, said isolation structure defining an area;

a buried oxide layer 5, 6, 7 formed between said bulk silicon substrate and said active layer, said buried oxide layer comprising a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate,

a first section 6 positioned between two second sections 5, 7, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section 6 being less than said thickness of said second sections 5, 7; and

said active layer being formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer, at least a portion of said channel region being positioned above said first section of said buried oxide layer. Inoue et al. do not teach a doped back gate region positioned at least partially in said bulk substrate under said multiple thickness buried oxide layer, wherein said doped back gate region extending under an entirety of said multiple thickness buried oxide layer between said isolation structure.

En et al. teach in figure 4A and related text a doped back gate region 38 positioned at least partially in said bulk substrate 76 under said buried oxide layer 72, wherein said doped back gate region extending under an entirety of said buried oxide layer and the area defined by said isolation structure 78.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a doped back gate region positioned at least partially in said bulk substrate under said multiple thickness buried oxide layer, wherein said doped back gate region extending under an entirety of said multiple thickness buried oxide layer between said isolation structure of Inoue et al.'s device in order to enhance the performance of the device when reducing the size of the device.

Regarding claims 10-11, 20-21, and 28-29, Inoue et al. teach in figure 2 and related text a transistor comprised of a gate electrode 8 and wherein said first section being substantially aligned with said gate electrode.

Regarding claims 4, 15 and 24, Inoue et al. teach in figure 2 and related text substantially the entire claimed structure, as applied to claims 1, 13 and 23 above, except using the device in at least one of a microprocessor, a memory device and a logic device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Inoue et al.'s device in at least one of a microprocessor, a memory device and a logic device, in order to use the device in an application which requires at least one of a microprocessor, a memory device and a logic device.

Regarding claims 6, 12, 17, 22, 26 and 30, Inoue et al. teach in figure 2 and related text substantially the entire claimed structure, as applied to claims 1, 13 and 23 above, except stating that said first section has a thickness ranging from approximately 30-50 nm, said second sections have a thickness ranging from approximately 120-180 nm, and said active layer has a thickness ranging from approximately 5-30 nm.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a first section having a thickness ranging from approximately 30-50 nm, second sections having a thickness ranging from approximately 120-180 nm, and an active layer having a thickness ranging from approximately 5-30 nm, in Inoue et al.'s device in order to adjust and optimize the device electrical characteristics, which depend on the thicknesses of the buried oxide layer and the thickness of the active layer.

Regarding claims 56-64 and 74-76, Inoue et al. teach in figure 2 and related text a transistor comprised of a channel region, said transistor comprising:

a bulk silicon substrate 1 and an active layer 2, 3, 4, said active layer 2, 4 being doped with a first type of dopant material;

a buried oxide layer 5, 6, 7 formed between said bulk silicon substrate and said active layer, said buried oxide layer comprising a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate, a first section positioned between two second sections, said first section

having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections;
said active layer formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer, at least a portion of said channel region being positioned above said first section of said buried oxide layer.

Inoue et al. do not teach a doped back gate region positioned at least partially in said bulk substrate under said buried oxide layer, wherein said doped back gate region being a doped region that is doped with a dopant material that is of the same type as said first type of dopant material.

En et al. teach in figure 3j and related text a doped back gate region 38 positioned at least partially on said bulk substrate 76 under said buried oxide layer 72, wherein said doped back gate region being a doped region that is doped with a dopant material that is of the same type as said first type of dopant material of the active layer 16, 18.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a doped back gate region positioned at least partially on said bulk substrate under said buried oxide layer of Inoue et al.'s device in order to enhance the performance of the device when reducing the size of the device.

Regarding the claimed limitations of a doped back gate region being a doped region that is doped with a dopant material that is of the same type as said first type of dopant material, these features are inherent in Inoue et al.'s device because although the doped back gate region is doped with a dopant material that is opposite to that of the

channel region, it has the same dopant material as that of the source/drain regions (which are part of the active layer).

Response to Arguments

Applicant argues that there is support in the disclosure for a device comprising an area defined by one (an) isolation structure formed in the active layer, as recited in claims 77-79, because the specification specifically notes that "trench isolation regions 17 are formed in the active layer 21 to electronically isolate the semiconductor device 10 from other semiconductor devices (not shown)", and it is well known that such isolation structures surround the transistor device to electronically isolate the transistor from other devices. Therefore, "those skilled in the art would readily understand how isolation structures work based upon the disclosure in the present application and the inherent knowledge of those skilled in the art".

The specification explicitly state that plurality of trench isolation regions 17 are formed in the active layer 21 to electronically isolate the semiconductor device 10 from other semiconductor devices. Therefore, although one trench isolation region can theoretically be formed to electronically isolate the semiconductor device 10 from other semiconductor devices, there is no support for one isolation structure surrounding the transistor device, as argued by applicant.

Applicant argues that "the use of the plural term "regions" is a consequence of the cross-sectional depiction of the semiconductor device 10, which results in portions

of the trench isolation region 17 appearing on opposite sides of the semiconductor device 10. This does not, however, indicate that the trench isolation region 17 is necessarily formed of multiple elements".

The specification states that "trench isolation regions 17 are formed in the active layer 21 to electronically isolate the semiconductor device 10 from other semiconductor devices (not shown)". This means that plurality of trench isolation regions 17, and not one trench, are formed in the active layer 21. In fact, this statement teaches away from a device comprising "a trench isolation region 17 surrounds the active layer 21 to electronically isolate the semiconductor device 10 from other semiconductor devices".

Applicant argues that there is support for the claimed limitations of "said doped back gate region extending under an entirety of said multiple thickness buried oxide layer between said isolation structure", as recited in claims 1, 13, 23 and 77-79, because "Figures 4A-4C of the present invention clearly show the back gate electrode 13 extending under the area defined by the isolation trenches 17".

The examiner agrees that figures 4A-4C of the present invention clearly show the back gate electrode 13 extending under the area defined by the isolation trenches 17. However, there is no support for the claimed limitations of "said doped back gate region extending under an entirety of said multiple thickness buried oxide layer between said isolation structure", as recited in claims 1, 13, 23 and 77-79.

Applicant argues that En et al. do not teach a doped back gate region extending under an entirety of said buried oxide layer between said isolation structure, because

En et al. teach a strip which extends along the width of the channel and does not extend under the source and drain regions.

Figure 4A of En et al. depicts a doped back gate region 38 extending under an entirety of said buried oxide layer between isolation structure 78. That is, the entirety of the doped back gate region, which is located under the buried oxide layer between said isolation structure, is depicted in figure 4A of En et al. The presence of the doped back gate region in other areas under the buried oxide layer is not required by the claims.

Furthermore, the location of the doped back gate region in figure 4A of En et al. is identical to the location of the doped back gate region in figure 4A of the claimed invention. Note that there is no support in the specification for the doped back gate region being located in other areas under the buried oxide layer.

Moreover, the broad recitation of the claim does not require the doped back gate region to extend under the source and drain regions or to extend beyond the outer edges of the polysilicon gate.

Applicant argues that En et al. do not teach a doped back gate region being doped with a dopant material that is of the same type as said first type of dopant material.

Although the doped back gate region of En et al. is doped with a dopant material that is opposite to that of the channel region, it has the same dopant material as that of the source/drain regions (which are part of the active layer).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
3/7/2008

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